Boundary-Scan Without Boundaries

Boundary-Scan Test Fundamentals
Including Design and Layout Considerations
Implementing Boundary-Scan Into Your PCB Designs

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Presentation Outline

• JTAG Test Fundamentals
• DFT – Schematic Design Guidelines
• DFT – Layout Design
• Q&A
IEEE 1149.1 Standard

- Developed during the late 80s
- Officially standardized in 1990
- BSDL language added in 1994
- Latest standard is maintained by IEEE:
  - Active Document name
    1149.1-2001: IEEE standard test access port and boundary-scan architecture
  - Publication Date: 2001
  - Page(s): i-200
  - Year: 2001
  - Contact
    1-800-678-4333 (USA and Canada)
    1-732-981-0060 (Worldwide)
    http://www.ieee.org
Increased Demand for JTAG

- PC boards are becoming more complex
  - Loss of physical/electrical access decreases effectiveness of Bed of Nails test technologies
  - Smaller, multilayer, internal vias, dual-sided placement, BGAs, more complex devices
- Product life cycles are becoming shorter
  - Minimize time from design to volume manufacturing
- Device packaging density and lack of access makes physical access
  - Expensive
  - Unreliable
  - Impossible
Boundary-Scan Architecture

The IEEE-1149.1 standard defines test logic in an integrated circuit which provides applications to perform:

- Chain integrity testing
- Interconnection testing between devices
- Core logic testing (BIST)
- In-system programming
- In-Circuit Emulation
- Functional testing
JTAG Chip Architecture

Major Building Blocks of JTAG Devices

- Test Data Registers
- Instruction Register
- TAP Controller
- JTAG Pins
JTAG Scan-Chain

TMS & TCK are connected in parallel
JTAG Test Vectors

Stimulus | Response
---|---
10001 | H L L L L
10010 | H L L L L
10100 | H L H L L
11000 | H H H H H

Short
Open
JTAG Benefits

- JTAG provides the capability to test interconnects on a PC-board without physical test probes or test fixtures
- Does not require the board to be in a bootable state for fault diagnostics
- JTAG allows In-System Programming of devices such as Flash, CPLDs, FPGAs and Serial EEPROMs
JTAG Advantages

• Automatic test generation removes engineers from having to create elaborate test cases
• Fast test times
• Net/Pin level diagnostics
• JTAG helps identify board problems up front meaning general purpose tools like oscilloscopes and voltage meters are used less
• Test vectors can be reused in production
Design For Test

Schematic Design Considerations

• JTAG Device Identification
• Scan-Chain Design
• TAP Interface Connector
• Board-Level DFT Design
JTAG Device Selection / Identification

- Datasheet indicates IEEE-1149.1, JTAG or boundary-scan compliance
- High pin count BGA or surface mount device (FPGA, CPLD, CPU, DSP)
- Pin names TCK, TMS, TDI, TDO and TRST_N
- BSDL file available
- Chip vendors such as Altera, AMCC, Atmel, Broadcom, Cypress, Freescale, IDT, Lattice, Marvell, Micron, National Semiconductor, QLogic, Samsung, ST Microelectronics, TI, Xilinx, and more
Scan-Chain Design

- Maximum testability is achieved when all JTAG devices are in one single chain

- This is because all JTAG devices are tested simultaneously in the serial chain
Scan-Chain Design

• Multiple scan-chains can be combined externally through hardware controllers

TDI1 \(\rightarrow\) U1 \(\rightarrow\) U2 \(\rightarrow\) TDO1

TDI2 \(\rightarrow\) U3 \(\rightarrow\) U4 \(\rightarrow\) U5 \(\rightarrow\) TDO2

TDI3 \(\rightarrow\) U6 \(\rightarrow\) U7 \(\rightarrow\) U8 \(\rightarrow\) TDO3

• Scan-chains can also be combined using cables or fixtures, but are often not as reliable
Scan-Chain Design

Scan Chain Debug Access & Test Points

- JTAG Connector
- TDI
- TCK
- TMS
- TDO

- JTAG
- Bypass Resistor

- Normally Installed (Uninstall to Bypass)
- Normally Uninstalled (Install to Bypass)

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Scan-Chain Design

Problematic components can be physically removed from the scan-chain. TMS should be pulled high.
Scan-Chain Design

- Check devices for full JTAG compliance
  - Identify up front whether devices have BSDL files available and ensure they have been tested
  - Some devices support emulation only or ISP only and cannot be utilized for interconnect tests. Information is often found in datasheets, device errata and BSDL files.

- Group components with similar voltage levels
  - Utilize a multi-TAP controller for programmable voltage interfacing or add voltage level shifting components to the design

- Always consider signal loading on the common signals TCK and TMS
  - Add TCK and TMS buffering on target when driving a large number of JTAG devices (recommend when more than 6)
Scan-Chain Design

- Dedicate a schematic page for a block diagram of the JTAG scan-chain
TAP Interface Connector

- Recommend Corelis TAP pin-out for robust one-to-one connection between the JTAG controller and the target
  - Every other pin is ground on cable providing improved signal integrity and noise immunity
- A solid ground is very important
- JTAG signal termination
- Multiple TAP connectors
  - Group by IC vendor
  - Group by voltage
  - Group by maximum device speed
  - Group by devices that requires different TCK / TRST_N termination
  - TMS, TCK, TRST_N signal fan out
  - Chain isolation debug
TAP Interface Connector

The 33 ohm resistor should be placed physically close to the device pin that drives this signal.

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TAP Interface Connector

Connector types

– Although different pinouts, most vendors use standard 0.1” x 0.1” pitch headers
– Shrouded header recommended to prevent incorrect insertion
– 2mm
– 0.050” x 0.050”
– Test points for fixture probe access
– Edge connectors
– Backplane
Board-Level Design

• Design boundary-scan into the product, not as an afterthought
  – Design engineers should think ahead about testing
  – Utilize DFT guidelines prior to and during board layout
• Consider initial power-up or reset state of board
• Ensure scan-chain is operational when power is applied
  – Properly terminate compliance enable pins
  – CPLDs that control power logic or scan-chain paths must remain in BYPASS
  – TRST_N pins must be high for JTAG testing
  – Constraints cannot be used if the scan-chain is not working
Board-Level Design

• Tri-state or disable non-boundary-scan devices
  – Provide boundary-scan control to disable device outputs that will otherwise conflict with nets involved in boundary-scan test (enable pins, test pins, reset signals, power shutdown circuitry)

• Disable these devices by:
  – Connecting a boundary-scan controllable output on the net to control the chip enable of the conflicting device (FIXED_HIGH, FIXED_LOW constraint)
  – Installing a dedicated jumper which put the target into a boundary-scan ready state
  – Connecting a GPIO pin available on the JTAG controllers to the offending net
Board-Level Design

• Considerations for memory cluster testing
  – Memory cluster tests are performed by controlling the pins on the memory device using surrounding JTAG logic including address pins, data pins, chip select/enable, output enable, RAS (DRAM), CAS (DRAM), clock (synchronous devices), write strobe (FIFO), read strobe (FIFO), and write enable
  – The driving boundary-scan devices must have separate control cells for the address, data, and control pins on the memory device
    • Although rare, some CPU devices have shared control cells
    • The BSDL file contains control cell information
Board-Level Design

• Considerations for memory cluster testing
  – JTAG control of the clock signals must be provided
    • Ensure the clock pin has a JTAG output cell to drive the clock
    • Linkage pins identified in the BSDL file cannot drive test patterns
    • If a PLL is used to drive the clock, ensure the PLL has a bypass feature that can be used during JTAG testing
    • The PLL bypass feature should be controllable using JTAG
      – Note some PLLs enable bypass by grounding the AVDD pin
    • Adding stubs to the clock net may alter the functional operation of the circuit
    • Memories can be functionally tested at-speed if they are connected to a supported EJTAG CPU
Board-Level Design

- Xilinx and Altera FPGA Considerations
  - Xilinx and Altera FPGA devices have different test characteristics depending on if the devices are configured
  - Maximum testability on these devices is in the pre-configuration state
  - To keep Xilinx parts in pre-configuration mode, the INIT* pin needs to be held low prior to and during power-up of the target
  - To keep Altera parts in pre-configuration mode, the NCONFIG* pin needs to be held low prior to and during power-up of the target
  - Recommend these pins route to the TAP header in place of a ground pin. When the JTAG controller plugs into the TAP, the pin will automatically be pulled low
Board-Level Design

FPGA Considerations

Target Board

Route to FPGA INIT* or NCONFIG* pins

To all Boundary Scan Devices
To TDI of 1st Device in the chain
From TDO of last Devices in chain
To all Boundary Scan Devices
To all Boundary Scan Devices

TRST*
TDO
TMS
TCK

1 2
3 4
5 6
7 8
9 10
Board-Level Design

• Compliance Enable Pins Must Be Satisfied
  – Compliance pin states are listed in the BSDL file
  – Correct compliance pin states must be maintained prior to and during JTAG testing to maintain test compliance
  – For example, the BSDL file for the Motorola MPC106 device describes the following compliance enable pin:

    attribute COMPLIANCE_PATTERNS of mpc106: entity is "(LSSD_MODE_L) (1)";

    indicates that pin LSSD_MODE_L must be a logic high prior to and during boundary-scan testing for correct JTAG operation
Board-Level Design

• Considerations for Flash In-System Programming
  – In-system programming of flash devices through JTAG is done by emulating read & write cycles to the flash device using surrounding JTAG logic including address pins, data pins, chip enable, output enable, write enable, and optionally reset, write protect and ready/busy
  – The driving boundary-scan devices must have separate control cells for the address, data, and control pins on the memory device
  – To reduce programming time:
    • Utilize boundary-scan devices with faster TCK rates
    • Ensure that your scan-chain is short
    • Remove unnecessary constraints
    • Use external write strobe (GPIO controlled)
Board-Level Design

- External Write Strobe (Flash In-System Programming)
  - The WRITE_STROBE* signal is active low and should be pulled high with a 1K resistor on the target board. It should be logically AND-ed with the WRITE_ENABLE* signal so that assertion of either the WRITE_ENABLE* signal or the WRITE_STROBE* signal will assert the flash WE* pin.
Board-Level Design

Flash In-System Programming Theoretical Speed Formula

\[
(#\text{bits in chain}) \times (#\text{scans/write}) \times (#\text{writes/location}) \times (#\text{locations})
\]

TCK frequency

Where:

- **#bits in chain** - effective length of the boundary-scan chain (assuming unused components placed in BYPASS)
- **#scans/write** - number of DR scans which are required in order to write a data value to the flash
- **#writes/location** - number of data values that must be written to program each location
- **#locations** - number of data locations to be programmed
- **TCK frequency** - frequency of the JTAG TCK signal
Design For Test

PCB Layout Considerations

• General
• Component Placement
• Trace Routing
• Test Points
• Multiple Scan-Chains
General

- TCK needs to be as free as possible of glitches and spikes, since all operations are triggered by rising and falling TCK edges.
- Connection of TDO of last device in scan chain to board TDO should be as short as possible.
- TCK and TMS fan out to every device is most critical.
- When using fan out buffers to distribute TCK, TMS and TRST_N, put termination resistors on the primary side of the buffer (signals coming from the JTAG controller).
- A serial resistor on the TDO of the last device in the chain should be close to that device’s TDO pin.
Component Placement

- Provide adequate room around the TAP connector to plug the cable in
  - Consider cable access when the product is enclosed or fully assembled
- Easier debug access when termination resistors are placed consistently close to the TAP connector along with a clearly labeled ground point
- Do not place the TAP connector near noisy analog components such as voltage regulators
- Consider access to probe the scan-chain when things don’t work
- Place JTAG devices such that a star topology can be implemented on the JTAG signals
Trace Routing

• Recommend general documented layout guidelines such as
  – A Practical Guide to High-Speed PCB Layout, Analog Devices
  – Guidelines for Designing High-Speed FPGA PCBs, Altera
  – High-Speed Board Layout Guidelines, Altera
  – Basic Principals of Signal Integrity, Altera
• Recommend JTAG traces be a minimum 10 mil width with minimum 10 mil spacing with length as short as possible
• JTAG signals should be routed on the outer layers away from noisy analog voltage regulators
• TMS and TCK are broadcast lines. They should be routed in accordance to high-frequency bus rules. Use fan out buffers to avoid overload of TMS and TCK signals coming from the JTAG controller.
• Route TCK and TMS in a star topology
• Signal quality is a key factor for successful JTAG testing
  – JTAG test signals should be assigned as critical for first pass route
  – Most common problems are reflections and ringing on TCK
  – Faster TCK results in faster in-system programming times
Test Points

- Compliance enable pins should be accessible. It is a good idea to place pads for both pull-up and pull-down resistors on the pin when in doubt.
- Even though TDI and TDO are point to point, consider an accessible test point at each link for debug if required.
- Always ensure there are convenient test point locations for ground.
  - Debug is much easier with the ability to clip one lead to ground.

Multiple Scan-Chains

- A working scan-chain should be one of the highest priorities.
- Breaking up a scan-chain may provide easier debug capability.
- Different groups use the JTAG chain differently.
  - Designers need JTAG for in-circuit emulation and in-system programming.
  - Test engineers need JTAG for interconnect testing.
Corelis Free Services

• Monthly Boundary-Scan Training
• DFT Guidelines Application Note
• DFT Analysis and Test Coverage Report

www.corelis.com
562-926-6727
Questions & Answers